AMENDMENT TO THE DRAWINGS

Please substitute the informal drawings filed with the original application with the enclosed, formal replacement sheets.

REMARKS

This Amendment is in response to the Office Action dated January 13, 2005, in which claims 13-28 were allowed, claims 3-10 were indicated as being allowable if rewritten in independent form, and claims 1-2, 11 and 12 were initially rejected. Applicants would like to thank the Examiner for the indicated allowability of claims 3-10 and 13-28 and respectfully request reconsideration of all remaining claims in view of the above-amendments and the following remarks.

I. AMENDMENT TO THE SPECIFICATION

The specification is amended as suggested in the Office Action to update the status of the copending application, which has now issued.

II. DRAWINGS

With this Amendment, Applicants submit formal replacement sheets for the informal drawings submitted with the original application. Acceptance of the replacement sheets is respectfully requested.

III. CLAIM REJECTIONS

Claims 1-2 and 11-12 were rejected under §102(e) as being anticipated by Lembach et al., U.S. Patent No. 4,698,760. Independent claim 1 of the present application is directed to a method of optimizing a functional block within a netlist. Corresponding delay values are assigned to a plurality of pins of the block, wherein each pin corresponds to a respective signal path through the block. These delay values together form a delay value combination that is selected from a continuous set of possible combinations in which each combination in the set satisfies a predetermined criteria. A circuit configuration is generated for the block with a plurality of logic cells that are interconnected in the netlist such that the respective signal paths through the block have delays based on the corresponding delay values that were assigned above.

In contrast, Lembach et al. disclose a method of optimizing the signal timing delays and power consumption in LSI circuits. As described in columns 5 and 6, Lembach et al. iterate a plurality of power levels and calculate respective time delays through each logic block for the respective power level. Based on these calculations, circuit logic blocks are set to different power levels. (See e.g., column 8, lines 46-57). As described in column 13, lines 64-67, the iterative method steps are performed until such time as no further performances changes occur and, no negative slacks exist in any of the circuit blocks. As described in column 14, lines 1-8, if negative slacks still exist, "it must be concluded that the technology of the circuit design cannot support the specified timing requirements which are imposed upon the overall network." In this case, Lembach et al. suggest "either a timing requirement modification must be made, or a logic design change must be made or a technology change must be made to another form of circuit."
In other words, Lembach et al. suggest that the method disclosed in his patent application "gives up" and leaves it to the logic designer to change the timing requirements, logic design, or technology outside of the disclosed method.

Lembach et al. clearly do not disclose "generating a circuit configuration for the block with a plurality of logic cells that are interconnected in the netlist such that the respective signal paths through the block have delays based on the corresponding delay values assigned in step (a)," as recited in claim 1. In the method disclosed in Lembach et al., the circuit configuration remains fixed. Only the power levels are changed.

Further, Lembach et al. does not disclose assigning delay values, "wherein the delay values together form a delay value combination that is selected from a continuous set of possible combinations in which each combination in the set

satisfies a predetermined criteria," as further recited in claim 1. Rather, Lembach et al. simply increment through various power levels and calculate timing delay.

Since Lembach et al. do not disclose each and every element of independent claim 1, Applicants respectfully request that the rejection of claim 1 and its dependent claims 2 and 11-12 under §102(e) based on Lembach et al. be withdrawn.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123.

Respectfully submitted,

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